Montgomery County Community College
CIS 126
Computer Architecture & Organization
3-2-2

COURSE DESCRIPTION:
This course is designed to explore how a computing system works and introduces the student to the organization and architecture of computer systems using the Assembly programming language. Computer Science students will gain insight into the functional components of a computer system. Topics covered will include digital logic, data representation, interfacing and I/O strategies, memory architecture, a computer's functional organization, and multiprocessing. The importance of CPU clock speed, cache size, bus organization, and number of core processors will also be discussed.

REQUISITES:
Previous Course Requirements

- CIS 111 Computer Science I: Programming and Concepts with a minimum grade of "C"

Concurrent Course Requirements
None

LEARNING OUTCOMES Upon successful completion of this course, the student will be able to:	LEARNING ACTIVITIES	EVALUATION METHODS
1. Design a simple circuit utilizing digital logic.	Lecture Discussion Projects Tests	Quizzes
2. Discuss data compression, rounding errors, and the limitations of representing data in digital form.	Lecture Discussion	Competency Checklist Live Computer Lab Demonstration
3. Trace the progression of computers from vacuum tubes to VLSI.	Lecture Discussion	Exams

LEARNING OUTCOMES	LEARNING ACTIVITIES	EVALUATION METHODS
4. Describe the architecture of a computer by defining the relationship between instruction set architecture, micro architecture, and system architecture.	Lecture Discussion	Competency Checklist
5. Define instruction set architecture (ISA), machine-level instruction in terms of its functionality and resource use (registers and memory) and the difference between register-to-memory ISAs and load/store ISAs.	Lecture Discussion Homework Assignments	Live Computer Lab Demonstration Exams
6. Distinguish between the various classes of instruction: data movement, arithmetic, logical, and flow control.	Lecture Discussion	Competency Checklist
7. Implement Assembly language code to demonstrate how subroutines are called, parameters are passed, and returns are made.	Lecture Discussion Hands-On Lab Exercises Homework Assignments	Live Computer Lab Demonstration Quizzes
8. Explain open- and closed-loop communications, the use of buffers to control dataflow and how interrupts are used to implement I/O control and data transfers.	Lecture	Competency Checklist Quizzes

LEARNING OUTCOMES	LEARNING ACTIVITIES	EVALUATION METHODS
9. Define various types of buses in a computer system and show how devices compete for and access is granted to a bus.	Lecture	Exams
10. Outline the progress in bus technology, memory technology and storage standards.	Lecture Discussion	Competency Checklist
11. Explain memory hierarchies, cache refill traffic, cache memory organization and cache coherency in multiprocessor systems.	Lecture Discussion	Quizzes
12. Implement register transfer language to show internal operations in a computer.	Lecture Hands-On Lab Exercises Discussion Homework Assignments	Live Computer Lab Demonstration
13. Illustrate how a CPU's control unit interprets a machine-level instruction and how conditional operations are implemented at the machine level.	Lecture Discussion	Live Computer Lab Demonstration
14. Chart the difference between processor performance and system performance. (i.e., the effects of memory systems, buses and software on overall performance)	Lecture Discussion	Competency Checklist

LEARNING OUTCOMES	LEARNING ACTIVITIES	EVALUATION METHODS
15. Describe superscalar architectures that use multiple arithmetic units to execute more than one instruction per clock cycle.	Lecture Discussion	Quizzes
16. Explain performance measurement limitations when using MIPS or SPECmarks.	Lecture Discussion	Live Computer Lab Demonstration
17. Analyze the relationship between power dissipation and computer performance and the need to minimize power consumption in mobile applications.	Lecture Discussion	Quizzes
18. Describe techniques used to enhance processor performance such as parallelism, pipelining, 64-bit register parallel processing of multimedia values, incorporating multiple processors on a single chip, and the use of special-purpose graphics processors, GPUs, for graphics applications.	Lecture Hands-On Lab Exercises	Live Computer Lab Demonstration Exams

At the conclusion of each semester/session, assessment of the learning outcomes will be completed by course faculty using the listed evaluation method(s). Aggregated results will be submitted to the Associate Vice President of Academic Affairs. The benchmark for each learning outcome is that *70% of students will meet or exceed outcome criteria*.

SEQUENCE OF TOPICS:

1. Digital Logic and Data Representation
    a. Introduction to digital logic (logic gates, flip-flops, circuits)
    b. Logic expressions and Boolean functions
    c. Representation of numeric data
    d. Signed and unsigned arithmetic
    e. Range, precision, and errors in floating-point arithmetic
    f. Representation of text, audio, and images
    g. Data compression
2. Computer Architecture & Organization
    a. Overview of the history of the digital computer
    b. Introduction to instruction set architecture, micro architecture and system architecture
    c. Processor architecture – instruction types, register sets, addressing modes
    d. Processor structures – memory-to-register and load/store architectures
    e. Instruction sequencing, flow-of-control, subroutine call and return mechanisms
    f. Structure of machine-level programs
    g. Limitations of low-level architectures
    h. Low-level architectural support for high-level languages
3. Interfacing and I/O Strategies
    a. I/O fundamentals: handshaking and buffering
    b. Interrupt mechanisms: vectored and prioritized, interrupt acknowledgment
    c. Buses: protocols, arbitration, direct-memory access (DMA)
    d. Examples of modern buses: e.g., PCIe, USB, Hypertransport
4. Memory Architecture
    a. Storage systems and their technology (semiconductor, magnetic)
    b. Storage standards (CD-ROM, DVD)
    c. Memory hierarchy, latency and throughput
    d. Cache memories – operating principles, replacement policies, multilevel cache, cache coherency
5. Functional Organization
    a. Review of register transfer language to describe internal operations in a computer
    b. Microarchitectures - hardwired and microprogrammed realizations
    c. Instruction pipelining and instruction-level parallelism (ILP)
    d. Overview of superscalar architectures
    e. Processor and system performance
    f. Performance – their measures and their limitations
    g. The significance of power dissipation and its effects on computing structures

6. Multiprocessing
   a. Amdahl's law
   b. Short vector processing (multimedia operations)
   c. Multicore and multithreaded processors
   d. Flynn's taxonomy: Multiprocessor structures and architectures
   e. Programming multiprocessor systems
   f. GPU and special-purpose graphics processors
   g. Introduction to reconfigurable logic and special-purpose processors

LEARNING MATERIALS:

- *Computer Organization and Architecture: Designing for Performance.* 10th Edition. Stallings, Prentice Hall. 2015. ISBN: 9780134101613.
- Learning materials, such as links to online Assembly Language programming resources, will be made available to the student via the course management system.

COURSE APPROVAL:

Prepared by:	Marie Hartlein	Date: 1995
Revised by:	Kathy Kelly	Date: 4/2012
Revised by:	Larry Elias	Date: 7/10/13
VPAA/Provost or designee Compliance Verification:		
	Victoria L. Bastecki-Perez, Ed.D.	Date: 7/11/2013

This course is consistent with Montgomery County Community College's mission. It was developed, approved and will be delivered in full compliance with the policies and procedures established by the College.